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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,774	11/21/2003	Shinichi Tanimoto	82478-2400	2894

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,774	TANIMOTO ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3 and 6-7 are rejected under 35 U.S.C. 102(e) as being unpatentable by Sasaki et al. (US Patent 6,546,528).

2. As to claims 1, 6 and 7 Sasaki discloses:

(1) A layout check system that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising (col.1, ll.9-14; col.5, ll.31-45):

a storage unit operable to store the layout- data (In step S12, the system stores the extracted layout information data to the storage block 13- col.8, ll.24-25, Figs.1 and 6), the layout data including information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second corresponding to impedance between the power pin and the bypass capacitor (... first and second impedance characteristics, being calculated by the calculator ... wherein the first impedance characteristic is calculated based on impedance of the power supply circuit being observed from a prescribed power terminal

connecting position, while the second impedance characteristic is calculated based on impedance of a selected circuit portion which lies from the prescribed power terminal connecting position to a capacitor arranged in most proximity to the prescribed power terminal connecting position on the printed-circuit board –claim 2) (col.8, ll.4-27; col.11, ll.29-38; col.11, ll.46-56; claim 2);

a calculation unit (Fig.6, block 12; Fig.7, steps S20 and S21) operable to calculate the first value and the second value, with use of the stored layout data (col.11, ll.29-38; col.11, ll.46-56; col.17, ll.48-50);

a judgment unit operable to judge (Fig.6, block 14; Fig.7, step S22), by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively (In step S22, the system compares first and second impedances previously calculated in steps 20 and 21) (col.11, ll.32-38; col.11, ll.55-56; col.18, ll.3-10); and

an output unit (Fig.6, block 4; Fig.7, steps S23) operable to output error information when a result of the judgment is negative (to represent occurrence of resonance and its resonance frequency ... the output device outputs the resonance information together with the first and second impedance characteristics as the evaluation information used for the evaluation of the electric characteristic of the printed-circuit board –col.18, ll.3-10) (col.4, ll.22-29; col.11, ll.57-67; col.12, ll.1-5; col.18, ll.3-10);

(6) A layout check method for checking layout data that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising (col.1, ll.9-14; col.5, ll.31-45):

a storage unit operable to store the layout- data (In step S12, the system stores the extracted layout information data to the storage block 13- col.8, ll.24-25, Figs.1 and 6), the layout data including information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second corresponding to impedance between the power pin and the bypass capacitor (... first and second impedance characteristics, being calculated by the calculator ... wherein the first impedance characteristic is calculated based on impedance of the power supply circuit being observed from a prescribed power terminal connecting position, while the second impedance characteristic is calculated based on impedance of a selected circuit portion which lies from the prescribed power terminal connecting position to a capacitor arranged in most proximity to the prescribed power terminal connecting position on the printed-circuit board –claim 2) (col.8, ll.4-27; col.11, ll.29-38; col.11, ll.46-56; claim 2);

a calculation unit (Fig.6, block 12; Fig.7, steps S20 and S21) operable to calculate the first value and the second value, with use of the stored layout data (col.11, ll.29-38; col.11, ll.46-56; col.17, ll.48-50);

a judgment unit operable to judge (Fig.6, block 14; Fig.7, step S22), by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively (In step S22, the system compares first and second

impedances previously calculated in steps 20 and 21) (col.11, ll.32-38; col.11, ll.55-56; col.18, ll.3-10); and

an output unit (Fig.6, block 4; Fig.7, steps S23) operable to output error information when a result of the judgment is negative (to represent occurrence of resonance and its resonance frequency ... the output device outputs the resonance information together with the first and second impedance characteristics as the evaluation information used for the evaluation of the electric characteristic of the printed-circuit board –col.18, ll.3-10) (col.4, ll.22-29; col.11, ll.57-67; col.12, ll.1-5; col.18, ll.3-10);

(7) A program that has a computer executable layout check processing that defines a layout of a power source, a component that includes a power pin, and a bypass capacitor on a printed wiring board, comprising (col.1, ll.9-14; col.5, ll.31-45):

a storage unit operable to store the layout- data (In step S12, the system stores the extracted layout information data to the storage block 13- col.8, ll.24-25, Figs.1 and 6), the layout data including information used for calculating a first value and a second value, the first value corresponding to impedance between the power pin and the power source, and the second corresponding to impedance between the power pin and the bypass capacitor (... first and second impedance characteristics, being calculated by the calculator ... wherein the first impedance characteristic is calculated based on impedance of the power supply circuit being observed from a prescribed power terminal connecting position, while the second impedance characteristic is calculated based on impedance of a selected circuit portion which lies from the prescribed power terminal

connecting position to a capacitor arranged in most proximity to the prescribed power terminal connecting position on the printed-circuit board –claim 2) (col.8, ll.4-27; col.11, ll.29-38; col.11, ll.46-56; claim 2);

a calculation unit (Fig.6, block 12; Fig.7, steps S20 and S21) operable to calculate the first value and the second value, with use of the stored layout data (col.11, ll.29-38; col.11, ll.46-56; col.17, ll.48-50);

a judgment unit operable to judge (Fig.6, block 14; Fig.7, step S22), by comparing the first value with the second value, whether the layout allows the bypass capacitor to function effectively (In step S22, the system compares first and second impedances previously calculated in steps 20 and 21) (col.11, ll.32-38; col.11, ll.55-56; col.18, ll.3-10); and

an output unit (Fig.6, block 4; Fig.7, steps S23) operable to output error information when a result of the judgment is negative (to represent occurrence of resonance and its resonance frequency ... the output device outputs the resonance information together with the first and second impedance characteristics as the evaluation information used for the evaluation of the electric characteristic of the printed-circuit board –col.18, ll.3-10) (col.4, ll.22-29; col.11, ll.57-67; col.12, ll.1-5; col.18, ll.3-10).

3. As to claims 2-3 Sasaki discloses:

(2) The layout check system of Claim 1, wherein the calculation unit calculates a shortest wiring distance (arranging in most proximity- col.17, ll.55-67; col.18, ll.1-10);

The layout check system of Claim 2, wherein a power via exists on wiring that connects the power pin and the bypass capacitor (col.8, ll.4-23; col.9, ll.35-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable by Sasaki 1 in view of Sasaki 2 et al. (US Patent 6,297,965).

With respect to claim 4 Sasaki 1 teaches the features above but lacks a layout check system/method/program defining a layout of a power source, a component including a power pin, and a bypass capacitor on a printed wiring board, wherein comparing step is based on a ratio of the first value to the second value.

5. As to claim 4 Sasaki 2 in view of Sasaki 1 recites:

a layout check system/method/program defining a layout of a power source, a component including a power pin, and a bypass capacitor on a printed wiring board, wherein comparing step is based on a ratio of the first value to the second value (Abstract; col.6, ll.35-58).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Sasaki 2's teaching regarding the layout check system/method/program defining a layout of a power source, a component including a

power pin, and a bypass capacitor on a printed wiring board, wherein comparing step is based on a ratio of the first value to the second value and use it in Sasaki 1's invention to create the characteristic impedance of a specific source line that is not less than three times as large as the impedance at an upper limit frequency at which the electromagnetic wave radiation of a specific capacitor may occur, thereby increasing an efficiency of suppressing the variation of the power source voltage and the radiation of the electromagnetic waves.

Allowable Subject Matter

6. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

a layout check system/method/program defining a layout of a power source, a component including a power pin, and a bypass capacitor on a printed wiring board further comprising an analysis unit to analyze using of a type information, whether wiring that connects the power pin and the bypass capacitor is a line or a plane; and a power plane judgment unit operable to judge, when a result of the analysis indicates that the wiring that connects the power pin is a plane, whether the surface area of the plane is less than the prescribed value, by referring to the area information, and when the surface area is less than the prescribed value, judge that the plane is a specific

power plane, and when the power plane judgment unit judges the wiring to be the specific power plan, the analysis unit further analyzes whether the specific power plane and the power source are connected without a bypass capacitor therebetween.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

STACY A. WHITMORE
PRIMARY EXAMINER